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Abstract
The new video coding standard recommendation H.264 of ITU-T, also known as International Standard 14496-10 or MPEG-4 Part 10 Advanced Video Coding (AVC) of ISO/IEC, has been developed. It significantly outperforms the previous ones (H.261, MPEG-1 Video, MPEG-2 Video, H.263, and MPEG-4 Visual or part 2) in the aspect of bit-rate reduction. At the same time, preliminary studies using software based on this new standard, suggest that H.264 offers up to 50% better compression than MPEG-2 and up to 30% better than H.263+ and MPEG-4 advanced simple profile. In the complexity simulation of H.264/AVC decoder/encoder, the deblocking filter is the most complexity part. Obviously to improve decoder/encoder performance, the deblocking filter will be considered first to be improved. In this thesis, we study and analyze deblocking filter in H.264/AVC. In order to reduce the number of memory references and thus improve overall system performance, we propose an advanced filtering process order with an efficient VLSI architecture which simultaneously processes the horizontal filtering of vertical edge and vertical filtering of horizontal edge. The processing capability of the proposed architecture is very appropriate for real-time deblocking of high-definition television (HDTV, 1920x1080 pixels/frame, 60 frames/video signals) video operation at 60 MHz. The proposed PBSR(Pipeline Buffer Shift Registers) and Window-based architecture deblocking filters are implemented by using Verilog HDL. The function of the implemented deblocking filters is also verified by ModelSim. It can be shown that the number of the total memory references is reduced by 78.75% and 52.5% respectively compared to the basic and advanced architectures of the previous works. As a result, the performance of our configurable window-based architecture with parallel engine significantly outperforms the previous designs in terms of memory references and processing cycles.
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