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Abstract
Read only memories (ROM) are often used to store constant data and play a major role in ASICs. However the designs of read only memories mostly adopt the full custom design method, there are relatively high for the designing period and cost. Against these shortcomings, we have designed a ROM compiler that can automatically generate the layout of a ROM according to the input of a ROM table. Our ROM compiler system includes two main parts; the compiler and the leaf cell library. In the design of complier, we have used PERL and SKILL languages to design the compiler. The compiler can analyze an input ROM table to decide the uses of leaf cells in the library to generate the layout, and therefore the performance of the ROM can be guaranteed to meet the specification of the design. In the design of leaf cells, we have partitioned the ROM circuit into five major parts: the row decoder, word-line buffer, core array, column decoder, and clocked buffer. In each part of the ROM circuit we have designed a number of leaf cells with different driving abilities by using the technology of TSMC 0.18 um. All the leaf cells in the library are designed and analyzed to meet the timing constraints, design requirements and design rules. Besides the DRC checking for a layout generated by our ROM compiler, we have performed LVS to confirm the correction of the design.
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