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Abstract
With the progress of the digital systems, the size of multimedia data, including images, audio and video signals, is increasingly large. Therefore, data compression is more and more extremely important and essential. For the development of multimedia compression and decompression technologies, the MPEG expert of ISO (International Standards Organization) has set the standards of storing and transmitting technologies for multimedia visual images , including MPEG-1 , MPEG-2 , MPEG-4, MPEG-7 and MEGP-21. Among these standards, MPEG-4 is mainly for the integration of telecomm- unication, computer and TV / films.
Because most of MPEG-4 encoders are implemented in software, the thesis implements the compression of MPEG-4 algorithms in the form of IP(Intellectual Property), named VCS (Video Coding System), and cooperates with X86 CPU to form an SOC (System On a Chip). To make VCS cooperate with CPU, an interface is designed to control data accessing between them. Besides, to reduce the number of operations of CPU and reach higher speed, all the access addresses will be calculated by the interface. Finally with practical operation of Xilinx Virtex2 FPGA, VCS uses nearly 1 million gates, and can operate at the speed of 35 MHz clock rate.
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