URN etd-0407109-183705-345
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Statistics This thesis had been viewed 80 times. Download 0 times.
Department
Year 2006
Semester 1
Degree Master
Type of Document Master's Thesis
Language zh-TW.Big5 Chinese
Title High Efficiency Self-Time 64-bit Comparators
Date of Defense 0000-00-00
Page Count 82

Keyword
asynchronous
comparators
high-speed
expandability
self-timed
dynamic logic

Abstract
The study on asynchronous circuit design had been years since mid-50's. Researchers on the study of asynchronous design have demonstrated the advantages of robustness, low power, and modularization. This paper presents a scheme for one of the fundamental arithmetic unit, the comparator, aiming for the advantages characterized above. This most-significant-bit comparator scheme is a key component for parallel testing, signature analyzer, and built-in self test circuits; therefore, the comparator design of ours is featured with high-speed in performance and expandability.
Our paper proposed structure for 64-bit parallel asynchronous comparator, which is implemented by dynamic CMOS logic with an empirical module of 2-bit comparator and a signal collector circuit with flexible adjustment when implement. The structure may be applied in all asynchronous system. We also implement it with TSMC 2P4M 0.35μm technology, and use the HSPICE to run the post-layout simulation and to demonstrate the enhancement with other known comparators.
Advisory Committee Yang Jung Lin - advisor

Files No Any Full Text File.
Date of Submission 2007-08-17