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Abstract
With the rapid development of semiconductor industry and the complicated of circuit design of the IC (Integrated Circuit), the size of the cell on a chip has become narrower to nanometer width. And the IC manufacture is toward to the goal of higher density, narrower line-width and lower cost. It must be improving the lithography technology in order to achieve the goals.
The layout design engineers only perform DRC (Design Rule Check) in layout they designed because of the layout design tool such as SpringSoft Laker / Cadense Virtuoso only to perform DRC in layout, and not perform LRC (Lithography Rule Check) in layout they designed.
So if we can not only perform DRC but also use the lithography simulator to get the aerial image on the wafer before the IC manufacturing process, and compare with the original layout to know the errors and distortions for the design. It can analysis the optical proximity effect for the design with the errors and distortions, then we can correct the layout and improve the yield and throughput for the design.
In this thesis, we developed an integrated system with existing EDA tools such that the photolithography simulator can be performed on the original layout.
The whole system can perform mask partition and polygon pattern decomposition in the original layout and integrated the format of GDSII with the input file of SPLAT simulator. So the RET (Resolution Enhancement Techniques) techniques like OPC (Optical Proximity Correction) to correct the original layout and improve the yield and throughput for the design.
In this thesis, two circuits, namely a DPLA (Dynamic Programable Logic Array) and a PLL (Phase-Locked Loop) are used for out experiments. The design flow from backend design to photolithograph simulator is successfully for these two circuits.
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