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Abstract
The Ultra Wideband (UWB) wireless communication is a linking option for the wireless personal area networks (WPANs). The multi-band orthogonal frequency division multiplexing (MB-OFDM) UWB is accepted by ISO and IEC as the standard of UWB system.The MB-OFDM UWB system employs the OFDM technology and the IFFT/FFT processor is the core of the OFDM processor. In this thesis, IFFT/FFT processor of a MB/OFDM UWB system is designed and presented. We propose a 128-point IFFT/FFT algorithm based on the Radix-16/8 pipeline architecture. The Canonic Signed Digit (CSD) algorithm is used to replace the multiplier inside the IFFT/FFT processor. The proposed IFFT/FFT processor will meet the requirement of the high data throughput rate, namely, the computation of 128-point FFT/IFFT will be done within 312.5 ns. The developed algorithms are shown to fulfill the requirements of the system specifications and are implemented by using Verilog hardware decription language (HDL). The proposed 128-point IFFT/FFT processor will be implemented by Xilinx FPGA (Field Programmable Gate Array) and its system perforamce is also verified.
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